The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.

Signed

Dated 25 April 2003

Patents Form 1/77

THE PATENT OFFICE
A
- 4 DEC 2002
NEWPORT

The Patent Office

040EC02 E768511-1 D00611 1/77
P01/7700 0.00-0228278.8

Patents Act 1977
Rule 16

Request for grant of a patent

The Patent Office
Concept House
Cardiff Road
Newport
South Wales NP10 8QQ

1.	Your reference	GB920020067GB1
2.	Patent application number *(The Patent Office will fill in this part)*	0228278.8
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	INTERNATIONAL BUSINESS MACHINES CORPORATION Armonk New York 10504 United States of America
	Patents ADP number *(if you know it)*	5196370001
	If the applicant is a corporate body, give the country/state of its incorporation	State of New York United States of America
4.	Title of the invention	AMPLIFIER ARRANGEMENT, CIRCUIT AND METHOD WITH IMPROVED COMMON MODE REJECTION RATIO
5.	Name of your agent *(if you have one)*	P Waldner
	"Address for Service" in the United Kingdom to which all correspondance should be sent *(including the postcode)*	IBM United Kingdom Limited Intellectual Property Department Hursley Park Winchester Hampshire S021 2JN
	Patents ADP number *(if you know it)*	7104417001

6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	Country	Priority App No *(if you know it)*	Date of filing *(day/month/year)*

7.	If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date or the earlier application	No of earlier application	Date of filing *(day/month/year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*
a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.)

Yes

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	7
Claim(s)	2 CF
Abstract	1
Drawing(s)	2 ~~+2~~

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	2
Request for preliminary examination and search *(Patents Form 9/77)*	
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application

Signature
P Waldner

3 December 2002
Date

12. Name and daytime telephone number of person to contact in the United Kingdom

P J Stretton
01962 815830

Patents Form 7/77

THE PATENT OFFICE
A
- 4 DEC 2002
NEWPORT

The Patent Office

7/77

Patents Act 1977
Rule 15

Statement of inventorship and of right to grant of a patent

The Patent Office
Concept House
Cardiff Road
Newport
South Wales NP10 8QQ

1.	Your reference	GB920020067GB1
2.	Patent application number *(if you know it)*	0228278.8
3.	Full name of the or of each applicant	INTERNATIONAL BUSINESS MACHINES CORPORATION
4.	Title of invention	AMPLIFIER ARRANGEMENT, CIRCUIT AND METHOD WITH IMPROVED COMMON MODE REJECTION RATIO
5.	State how the applicant(s) derived the right from the inventor(s) to be granted a patent	By employment and by agreement
6.	How many, if any, additional Patents Forms 7/77 are attached to this form?	
7.		I/We believe that the person(s) named over the page (and on any extra copies of this form) is/are the inventor(s) of the invention which the above patent application relates to. Signature P Waldner 3 December 2002 Date
8.	Name and daytime telephone number of person to contact in the United Kingdom	P J Stretton Tel: 01962 815830

Enter th ll names, addresses and postcodes of the inventors in the boxes and underline the surnames

Michael Alan VEAL
(UK resident)
c/o IBM United Kingdom Limited
Intellectual Property Law
Hursley Park
Winchester
Hampshire SO21 2JN
England

Patents ADP number *(if known)*
7805492001

Patents ADP number *(if known)*

If there are more than three inventors, please write their names and addresses on the back of another Patents Form 7/77 and attach it to this form

Patents ADP number *(if known)*

REMINDER

Have you signed the form?

AMPLIFIER ARRANGEMENT, CIRCUIT AND METHOD WITH IMPROVED COMMON MODE REJECTION RATIO

Field of the Invention

This invention relates to current sensing and particularly but not exclusively to load current sensing in load driver circuits.

Background of the Invention

In the field of this invention it is known that in a simple load driver circuit a differential amplifier is used to amplify a voltage across a current sense resistor carrying a load current.

Referring to FIG. 1, such a circuit is shown having an input node 10 and a ground node 20, between which there is an input voltage V_{IN}.

A high side current sense resistor 30 has a first terminal coupled to the input node 10, and a second terminal to be further described below.

An amplifier 40, which is a typical differential amplifier, has an inverting input coupled to the input node 10, a non-inverting input coupled to the second terminal of the resistor 30 and an output coupled to an output node 50.

In operation, a voltage V_1 is developed across the resistor 30. The voltage developed is proportional to the current I_{LOAD} flowing in the resistor 30. Ideally, the voltage V_1 should be insignificant compared to the input voltage V_{IN}. A voltage V_2 between the output node 50 and the ground node 20 is defined by:

$$V_2=A(V^+-V^-) \qquad \text{Equation 1}$$

Where A is the gain of the amplifier 40, V^+ is the voltage at the non-inverting input of the amplifier 40 and V^- is the voltage at the inverting input of the amplifier 40.

In the circuit shown, this may be written as:

$$V_2=A*V_1 \qquad \text{Equation 2}$$

This circuit works well in theory, and in practice at low frequencies. However, at high frequencies, the amplifier 40 will typically

have a low Common Mode Rejection Ratio (CMRR), and the output equation must be re-written to take this into account:

$$V_2 = A(V_1+V_{CM}/CMRR) \qquad \text{Equation 3}$$

where V_{CM} is any high frequency variation in the input voltage V_{IN}. If the CMRR is low, and the common mode voltage V_{CM} is large with respect to V_1, then any variation in V_{IN} will cause a large variation at V_2.

This is undesirable since the circuit is typically required to have an output equivalent to equation 1 above (namely an output which is linearly proportional to the circuit input voltage) over a large frequency range.

The problem has been addressed in a variety of ways. A standard "instrumentation amplifier" configuration uses three differential amplifiers and does not require precision components. However, an "instrumentation amplifier" arrangement requires higher precision components than are used in this invention. Furthermore, this invention may provide a better CMRR figure than an instrumentation amplifier when a high frequency common mode signal is applied.

EP1176711 A2 discloses a scheme for improving harmonic distortion within a differential amplifier.

US 6218901 B1 and US 6429700 B1 disclose methods of setting an output common mode voltage of an amplifier with a differential output.

A need therefore exists for an amplifier arrangement, circuit and method with improved CMRR wherein the abovementioned disadvantages may be alleviated.

Statement of Invention

In accordance with a first aspect of the present invention there is provided an arrangement with improved common mode rejection ratio in a load driver circuit having an input voltage and a ground voltage, the arrangement comprising: a voltage regulator adapted to regulate the ground voltage in response to variations in the input voltage and coupled to provide a regulated ground voltage; amplifier means including sense inputs coupled to receive voltage signals from a sense resistor of the load driver circuit, for providing an amplified output voltage; wherein the amplifier means is adapted to be powered by power terminals coupled to the input

voltage and the regulated ground voltage respectively, such that the common mode rejection ratio of the load driver circuit is reduced.

In accordance with a second aspect of the present invention there is provided a load driver circuit comprising an arrangement for providing an improved common mode rejection ratio in a load driver circuit having an input voltage and a ground voltage, the arrangement comprising: a voltage regulator adapted to regulate the ground voltage in response to variations in the input voltage and coupled to provide a regulated ground voltage; amplifier means including sense inputs coupled to receive voltage signals from a sense resistor of the load driver circuit, for providing an amplified output voltage; wherein the amplifier means is adapted to be powered by power terminals coupled to the input voltage and the regulated ground voltage respectively, such that the common mode rejection ratio of the load driver circuit is reduced.

In accordance with a third aspect of the present invention there is provided a method for providing an improved common mode rejection ratio in a load driver circuit having an input voltage and a ground voltage, the method comprising the steps of: regulating the ground voltage in response to variations in the input voltage in order to provide a regulated ground voltage; amplifying voltage signals received from a sense resistor of the load driver circuit using amplifier means, for providing an amplified output voltage; wherein the amplifier means is adapted to be powered by power terminals coupled to the input voltage and the regulated ground voltage respectively, such that the common mode rejection ratio of the load driver circuit is reduced.

Preferably the circuit is a high side driver circuit. The amplifier means preferably includes first and second differential amplifiers.

The first differential amplifier preferably has power terminals coupled to the input voltage and the regulated ground voltage respectively and the second differential amplifier preferably has power terminals coupled to the input voltage and the ground voltage respectively.

Preferably the first and second differential amplifiers each have gain values adapted to produce a circuit gain value of substantially unity. The second differential amplifier preferably has a non-inverting input coupled to an output of the first differential amplifier and an inverting input coupled to the regulated ground voltage.

In this way an arrangement, circuit and method is provided in which CMRR is drastically improved, rendering a single (or first) stage of a

current sensing load driver circuit substantially immune to common mode noise.

Brief Description of the Drawings

One amplifier arrangement, circuit and method with improved CMRR incorporating the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

FIG. 1 shows a block schematic drawing illustrating a prior art current sensing high side load driver circuit; and

FIG. 2 shows a block schematic drawing illustrating a current sensing high side load driver circuit with improved CMRR incorporating the present invention.

Description of Preferred Embodiment(s)

Referring to FIG. 2, there is shown a block schematic drawing of a current sensing high side load driver circuit according to the present invention.

The circuit has an input node 110 and a ground node 120, between which there is an input voltage V_{IN}.

A high side current sense resistor 130 has a first terminal coupled to the input node 110, and a second terminal to be further described below.

A first amplifier 140, which is a typical differential amplifier, has an inverting input coupled to the input node 110, a non-inverting input coupled to the second terminal of the resistor 130 and an output to be further described below.

A negative voltage three terminal linear regulator 150 has an input terminal coupled to the ground node 120, a ground terminal coupled to the input node 110 and an output terminal to be further described below.

The first amplifier 140 has a first power terminal coupled to the input node 110 and a second power terminal coupled to the output terminal of the regulator 150.

A second amplifier 160, which is a typical differential amplifier, has an inverting input coupled to the output terminal of the regulator 150, a non-inverting input coupled to output of the first amplifier 140 and an

output coupled to an output node 170. The second amplifier 160 has a first power terminal coupled to the input node 110 and a second power terminal coupled to the ground node 120.

In this way an arrangement using two differential amplifiers is used. The first amplifier 140 is powered via the input node 110 and a regulated ground voltage (by virtue of the regulator 150). The second amplifier is powered normally (that is, via the input node 110 and ground node 120).

In operation, the regulator 150 is used to maintain a voltage V_4 given by:

$$V_4 = V_{IN} - V_O \qquad \text{Equation 4}$$

where V_O is the output terminal voltage of the regulator 150.

For this circuit to operate correctly, the input V_{IN} may not swing lower than a value equal to V_O Volts plus the drop out voltage of the regulator 150.

This arrangement of power applied to the first amplifier 140 means that as the input voltage V_{IN} varies, then the first and second power supply terminals and the inverting and non-inverting inputs of the first amplifier 140 track V_{IN}.

The first amplifier 140 is therefore immune to variations in V_{IN}, and has no common mode input signal. The output equation for this stage may be written as:

$$V_2 = A_1 * V_1 \qquad \text{Equation 5}$$

Where A_1 is the gain of the first amplifier 140.

However V_2 is not equivalent to the output of FIG. 1 as the voltage V_2 is between the output of the second amplifier 140 and V_O (GND plus V_4), not GND.

This is why the second amplifier 160 is also used. It effectively subtracts the Voltage V_4 from V_2 and scales the output to the desired value.

Any variation in the input voltage V_{IN} now appears as a common mode input voltage V_{CM} for the second amplifier 160, and the equation for the output may be written as:

$V_3 = A_2(V_2 + V_{CM}/CMRR)$ Equation 6

Where A_2 is the gain of the second amplifier 160.

Equation 6 may be rewritten as:

$V_3 = A_2*A_1*V_1 + A_2*V_{CM}/CMRR$ Equation 7

The overall CMRR of the above circuit represents an improvement factor of $1/A_2$ in comparison with the prior art circuit of FIG. 1.

The following numerical example illustrates the advantage of the present invention:

V_{IN} varies between 6V and 12V
V_1 = 50mV
V_O may be set to 5V.

From equation 4 above, $V_4 = V_{IN} - V_O$, setting V_O to 5V means that V_4 is always positive by more than the drop out voltage of the regulator 150 (assumed to be less than 1V in this example).

A_1 = 5V/50mV = 100, to give the maximum gain for this stage.

$A_2 = 1/A_1 = 0.01$ to give a unity gain overall.

From equation 7 above, ($V_3 = A_2*A_1*V_1 + A_2*V_{CM}/CMRR$):

$V_3 = 100 * 0.01*V1 + 0.01*V_{CM}/CMRR$ Equation 8

Which can be rewritten as:

$V_3 = V_1 + V_{CM} * 0.01/CMRR$ Equation 9

In this way the CMRR is drastically improved, rendering a single (or first) stage of a current sensing load driver circuit to be substantially immune to common mode noise.

It will be appreciated by a person skilled in the art that alternative embodiments to those described above are possible.

For example, the numerical example mentioned above represents only one of the possible set of parameters for the above circuit. Furthermore, alternative arrangements are envisaged which may differ as to their

implementation details, but which are functionally equivalent to the embodiment described above.

CLAIMS

1. An arrangement for providing an improved common mode rejection ratio in a load driver circuit having an input voltage and a ground voltage, the arrangement comprising:

a voltage regulator adapted to regulate the ground voltage in response to variations in the input voltage and coupled to provide a regulated ground voltage;

amplifier means including sense inputs coupled to receive voltage signals from a sense resistor of the load driver circuit, for providing an amplified output voltage;

wherein the amplifier means is adapted to be powered by power terminals coupled to the input voltage and the regulated ground voltage respectively, such that the common mode rejection ratio of the load driver circuit is reduced.

2. A load driver circuit comprising the arrangement according to claim 1.

3. The load driver circuit of claim 2 wherein the circuit is a high side driver circuit.

4. A method for providing an improved common mode rejection ratio in a load driver circuit having an input voltage and a ground voltage, the method comprising the steps of :

regulating the ground voltage in response to variations in the input voltage in order to provide a regulated ground voltage;

amplifying voltage signals received from a sense resistor of the load driver circuit using amplifier means, for providing an amplified output voltage;

wherein the amplifier means is adapted to be powered by power terminals coupled to the input voltage and the regulated ground voltage respectively, such that the common mode rejection ratio of the load driver circuit is reduced.

5. The arrangement, circuit or method of any preceding claim wherein the amplifier means includes first and second differential amplifiers.

6. The arrangement, circuit or method of claim 5 wherein the first differential amplifier has power terminals coupled to the input voltage and the regulated ground voltage respectively and the second differential amplifier has power terminals coupled to the input voltage and the ground voltage respectively.

7. The arrangement, circuit or method of claim 5 or claim 6 wherein the first and second differential amplifiers each have gain values adapted to produce a circuit gain value of substantially unity.

8. The arrangement, circuit or method of any one of claims 5 to 7 inclusive wherein the second differential amplifier has a non-inverting input coupled to an output of the first differential amplifier and an inverting input coupled to the regulated ground voltage.

9. An arrangement substantially as hereinbefore described with reference to FIGS. 2 and 3 of the accompanying drawings.

10. A circuit substantially as hereinbefore described with reference to FIGS. 2 and 3 of the accompanying drawings.

11. A method substantially as hereinbefore described with reference to FIGS. 2 and 3 of the accompanying drawings.

ABSTRACT

AMPLIFIER ARRANGEMENT, CIRCUIT AND METHOD WITH IMPROVED COMMON MODE REJECTION RATIO

A load driver circuit is provided with an improved common mode rejection ratio. A voltage regulator (150) regulates a ground voltage (120) in response to variations in input voltage (110) and provides a regulated ground voltage. An amplifier stage has a first amplifier (140) with sense inputs coupled to receive voltage signals from a sense resistor (130) of the load driver circuit. The first amplifier (140) is powered by the input voltage (110) and the regulated ground voltage respectively, such that the common mode rejection ratio of the load driver circuit is reduced. In this way an arrangement, circuit and method is provided in which CMRR is drastically improved, rendering a single (or first) stage of a current sensing load driver circuit substantially immune to common mode noise.

FIG. 1
Prior Art

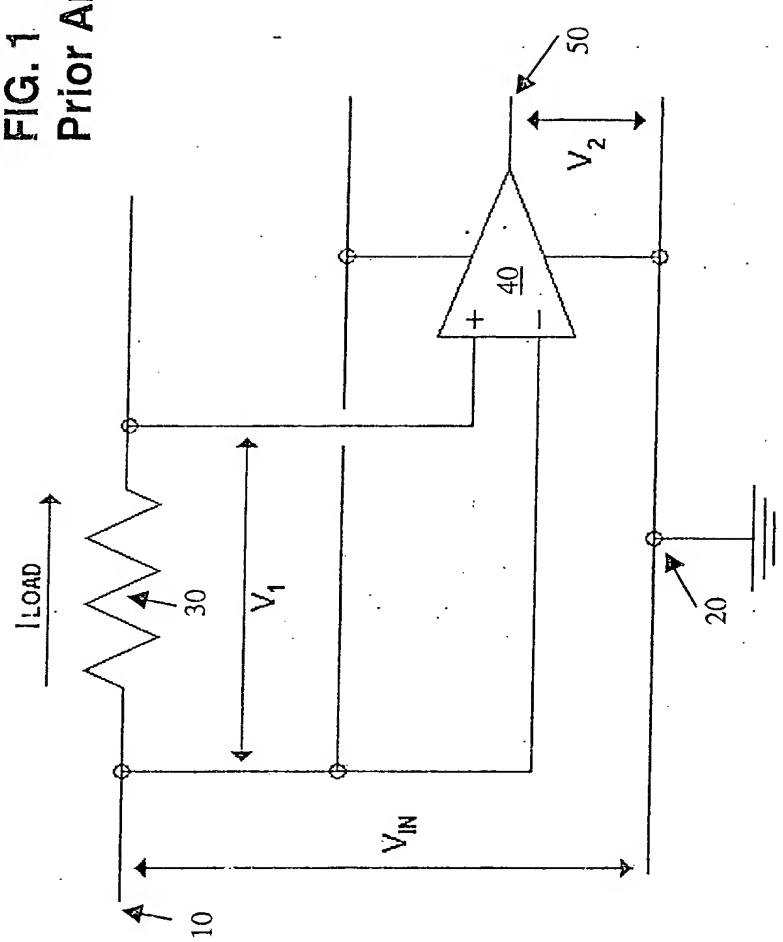

FIG. 2